MCS-96 MICRCONTROLLER

Introduction

The Intel MCS-96 (launched during 1982) is a family of 16-bit microcontrollers (MCU) commonly used in embedded systems. The family is often referred to as the 8xC196 family, or 80196, the most popular MCU in the family. These MCUs are commonly used in hard disk drives, modems, printers, pattern recognition and motor control.

The MSC-96 family members are all high performance microcontroller with a 16 bit CPU and atleast 230 bytes of on-chip RAM. Intel MSC-96 family easily handles high speed calculations and fast input/out operations. All of the MCS-96 components share a common instruction set and architecture. However the CHMOS components have enhancements to provide higher performance with lower power consumption. These microcontrollers contain dedicated I/O subsystem and perform 16-bit arithmetic instructions including multiply and divide operations. The major components of the MCS-96 CPU are the Register File and the Register / Arithmetic Logic Unit (RALU). Location 00H through 17H are the I/O control registers or Special function registers (SFR). Locations 18H and 19H contains the stack pointer, which can serve as general purpose RAM when not performing stack operations. The remaining bytes of the register file serve as general purpose RAM, accessible as bytes, words or double-words. Calculations performed by the CPU take place in the RALU. The RALU contains a 17bit ALU, the program status word (PSW), the program Counter (PC), a loop counter and three temporary registers. The RALU operates directly on the Register Files, thus eliminating accumulator bottleneck and providing for direct control of I/O operations through the SFR.

Features

- Frequency of Operation: 40 MHz
- 2 Mbytes of linear address space
- 1 Kbyte of register RAM
- 3 Kbytes of code RAM
- 8 Kbytes of ROM
- 2 peripheral interrupt handlers (PIH)
- 6 peripheral interrupts
- 83 I/O port pins
- 2 full-duplex serial ports with baud-rate generators
- Synchronous serial unit
- 8 pulse-width modulator (PWM) outputs with 8-bit resolution
- 16-bit watchdog timer
- Sixteen 10-bit A/D channels
- Programmable clock output signal

Architecture

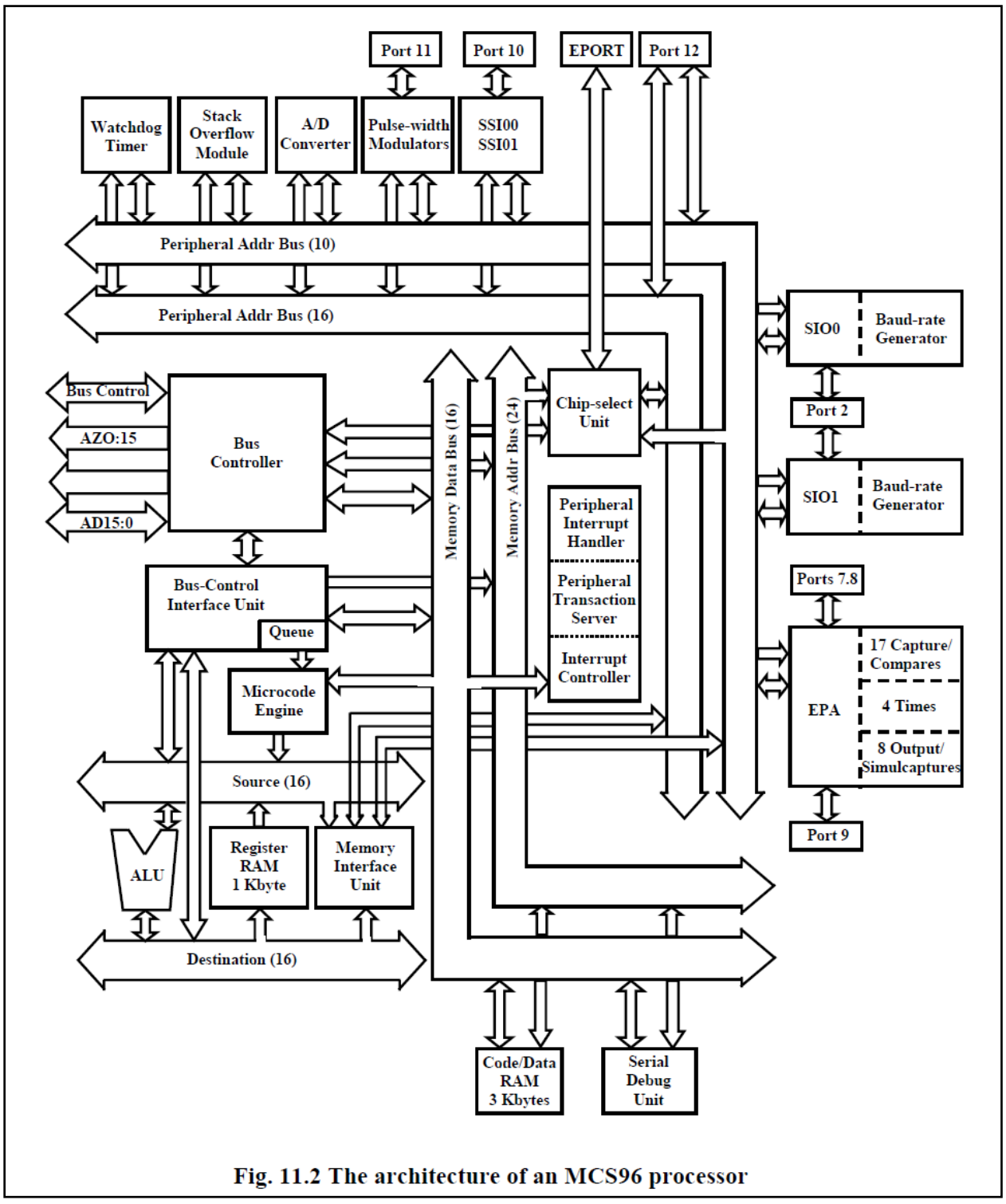

Fig. 11.2 The architecture of an MCS96 processor

The MCS-96 supports a complete instruction set which includes bit operations, byte operations, word operations, double-word operations (unsigned 32 bit), long operations (signed 32 bit), flag manipulations as well as jump and call instructions. All the standard logical and arithmetic instructions function as both byte and word operations. The jump bit set and jump bit clear instructions can operate on any of the SFR or bytes in the lower register files. These fast bit manipulations allow for rapid I/O functions. Byte and word operations make up the instruction set. The assembly language ASM-96 uses a “B” suffix on a mnemonic for a byte operation or for word operation.